CLAIMS

What is claimed is:

1. An I/O interface for an integrated circuit chip having a core, a pad, and a data buffer disposed between the core and the pad, the data buffer comprising:

an output circuit including:

a plurality of output latches, each output latch having at least one input coupled to receive output data signals from the core;

a plurality of output clock trees, each output clock tree coupled to at least one of the output latches for triggering the latching of the output data signals from the core, each output clock tree disposed in the I/O interface;

a first signal conditioning circuit coupled to the output latches for conditioning the output data signals so that the output data signals are compliant with at least one of a plurality of protocols;

an input circuit including:

a plurality of input latches, each input latch having at least one input coupled to receive input data signals from the pad;

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an input clock tree coupled to at least one of the input latches for triggering the latching of the input data signals from the pad; and

a second signal conditioning circuit coupled to the input latches for conditioning the input data signals so that the input data signals are compliant with at least one of the plurality of protocols.

2. The I/O interface of claim 1, wherein the input clock tree distributes to the data buffer a clock/strobe signal generated from a source external to the I/O interface.

3. The I/O interface of claim 1, wherein the output data signals and the input data signals are conditioned by the first signal conditioning circuit and the second signal conditioning circuit, respectively, to be compliant with a protocol that is selected on-the-fly.

4. The I/O interface of claim 3, wherein the protocol is selected from the group of protocols consisting of AGP, DDR/SSTL, and PCI/TTL.

5. The I/O interface of claim 4, wherein the data buffer operates in a synchronous mode for AGP and DDR/SSTL protocols, and the data buffer operates in an asynchronous mode for PCI/TTL protocol.

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6. The I/O interface of claim 1, wherein the output circuit includes a first output latch, a second output latch, and a third output latch, the first output latch and the second output latch each coupled to a first output clock tree, the third output latch coupled to a second output clock tree, the output clock trees for triggering the latching of the output data signals from the core in a synchronous manner.

7. The I/O interface of claim 6, wherein the first clock tree provides a double rate clock and the second clock tree provides a single rate clock.

8. The I/O interface of claim 6, wherein the first output latch, the second output latch, and the third output latch are edge-triggered flip-flops.

9. The I/O interface of claim 1, wherein the first signal conditioning circuit comprises:

a pre-driver having an input and an output, the input coupled to the output latches for receiving the output data signals;

a voltage tolerant circuit having an input and an output, the input coupled to the output of the pre-driver for receiving output data signals; and

a driver circuit having an input and an output, the input coupled to the output of the voltage tolerant circuit for receiving the output data signals, the output of the

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driver circuit coupled to the pad for providing a pad voltage compliant with one of the plurality of protocols.

10. The I/O interface of claim 9, wherein the voltage tolerant circuit is further coupled to the pad via a switching well, the switching well operating in conjunction with the voltage tolerant circuit and the driver circuit to compare the pad voltage with a supply voltage and switching the higher of the two voltages to the switching well.

11. The I/O interface of claim 10, wherein the switching well is further coupled to a pull-up/pull-down circuit for adjusting the pad voltage.

12. The I/O interface of claim 11, wherein the pull-up/pull-down circuit includes a pull-up resistor and a pull-down resistor, each resistor responsive to an enabling signal from the core.

13. The I/O interface of claim 1, wherein the input circuit includes a first input latch, a second input latch, and a third input latch, each input latch coupled to the input clock for triggering the latching of the input data signals from the pad in a synchronous manner.

14. The I/O interface of claim 1, wherein the input circuit includes a Schmitt trigger coupled to the pad for receiving input data signals compliant with PCI/TTL protocol.

15. The I/O interface of claim 1, wherein the input circuit includes a differential amplifier coupled to the pad for receiving differential input data signals.

16. An I/O interface for an integrated circuit chip having a core, a pad, and a clock/strobe buffer disposed between the core and the pad, the clock/strobe buffer comprising:

a differential amplifier having an input and an output, the input coupled to the pad for receiving differential clock/strobe signals complying with one of a plurality of protocols;

a programmable delay module having inputs and an output, a first input coupled to the output of the differential amplifier for receiving the clock/strobe signals, a second input for receiving a plurality of program bits for delaying the clock/strobe signals; and

a gated buffer coupled to the output of the programmable delay module and an input clock tree, the gated buffer for distributing the clock/strobe signals to the I/O interface via the input clock tree.

17. The I/O interface of claim 16, wherein the protocol is selected from the group of protocols consisting of AGP and DDR/SSTL.

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18. The I/O interface of claim 16, wherein the clock/strobe buffer further includes a Schmitt trigger coupled to the pad and the gated buffer for receiving TTL clock/strobe signals from the pad and distributing the TTL clock/strobe signals to the I/O interface via the input clock tree.

19. An I/O interface for an integrated circuit chip having a core, a pad, and a clock/strobe buffer disposed between the core and the pad, the clock/strobe buffer comprising:

an output circuit including:

an output latch having at least one input coupled to receive output clock/strobe signals from the core, the output latch coupled to a first clock tree for triggering the latching of the output clock/strobe signals from the core, the first output clock tree disposed in the I/O interface;

a multiplexer having at least one input coupled to a second clock tree, the multiplexer for reducing the skew on the clock/strobe signals, the second output clock tree disposed in the I/O interface;

a first signal conditioning circuit coupled to the output latch and the multiplexer for conditioning the output clock/strobe signals so that the output clock/strobe signals are compliant with at least one of a plurality of protocols;

an input circuit including:

a differential amplifier having an input and an output, the input coupled to the pad for receiving differential clock/strobe signals complying with one of a plurality of protocols; and

a gated buffer coupled to the output of the differential amplifier and an input clock tree, the gated buffer for distributing the clock/strobe signals via the input clock tree .

20. The I/O interface of claim 19, wherein the protocol is selected from the group of protocols consisting of AGP and DDR/SSTL.

21. The I/O interface of claim 19, wherein the clock/strobe buffer further includes a Schmitt trigger coupled to the pad and the gated buffer for receiving TTL clock/strobe signals from the pad and distributing the clock/strobe signals to the I/O interface via the input clock tree.